PCI Tutorial

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Agenda

PCI Fundamentals

- PCI Local Bus Architecture
- PCI Signals
- Basic Bus Operations
- PCI Addressing and Bus Commands
- PCI Configuration
- Electrical and Timing Specifications
- 64-bit Extension
- 66-MHz Overview
- PCI Variations

Xilinx PCI Solution

- The PCI Challenge
- Xilinx PCI with Design Examples
- Xilinx PCI Design Flow Overview
- Available Resources

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PCI Fundamentals and Concepts

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PCI Local Bus Architecture

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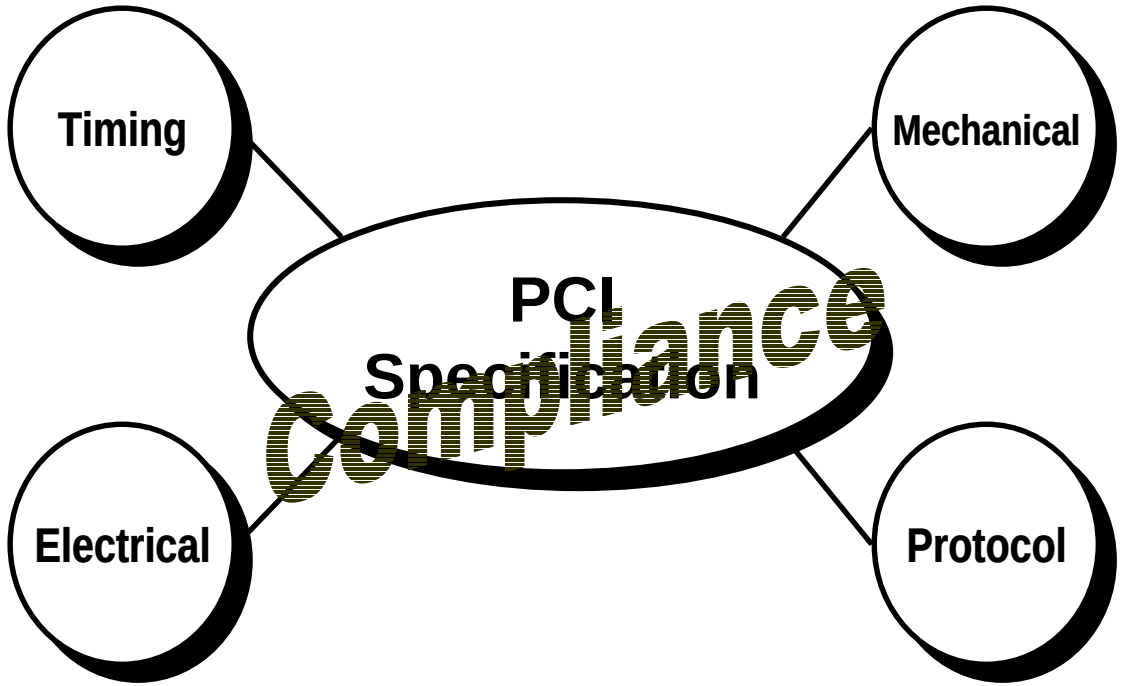
Overview of the PCI Specification

- ***The PCI Local Bus Specification*** **covers many different requirements for PCI compliance**



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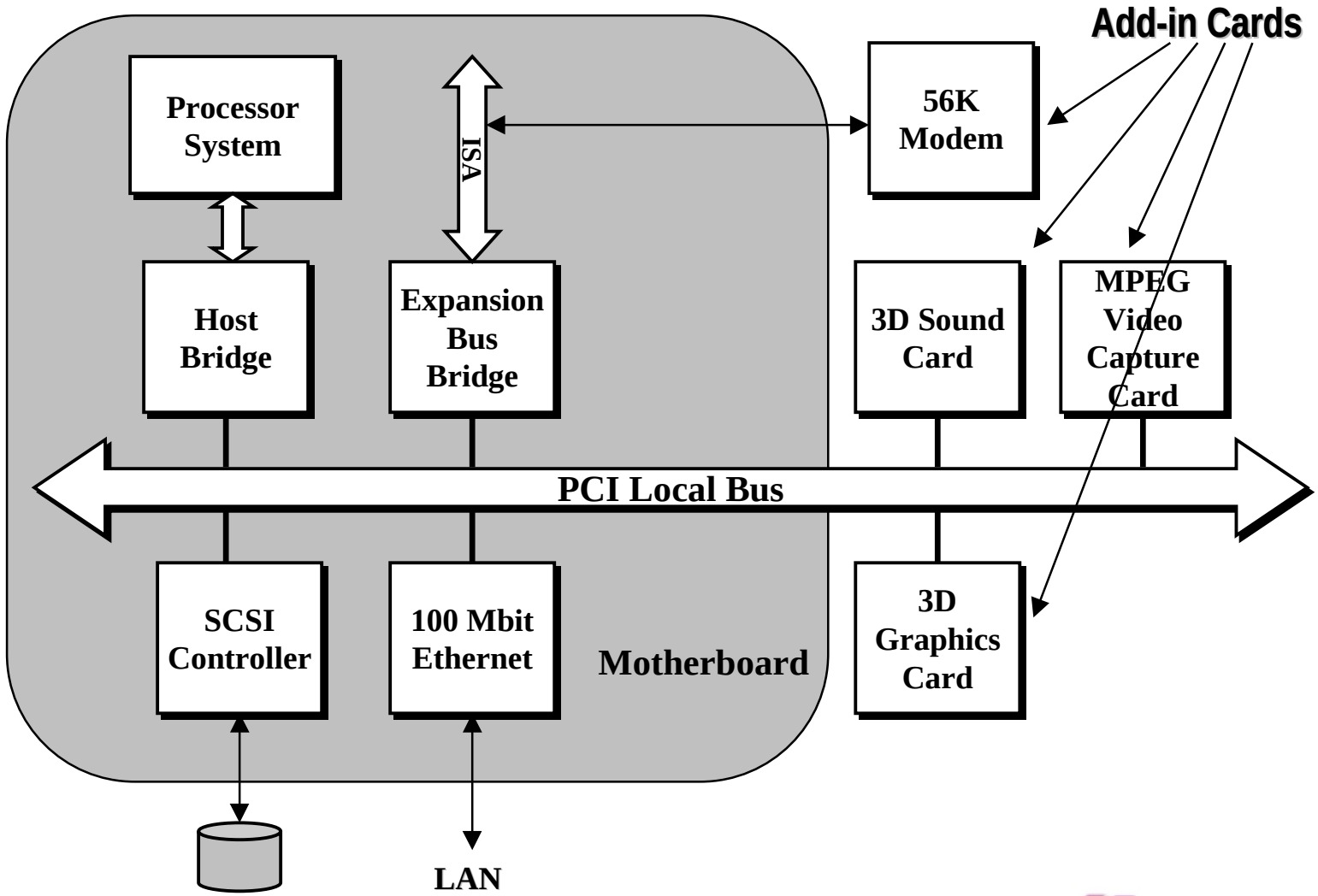
Basic Bus Architecture



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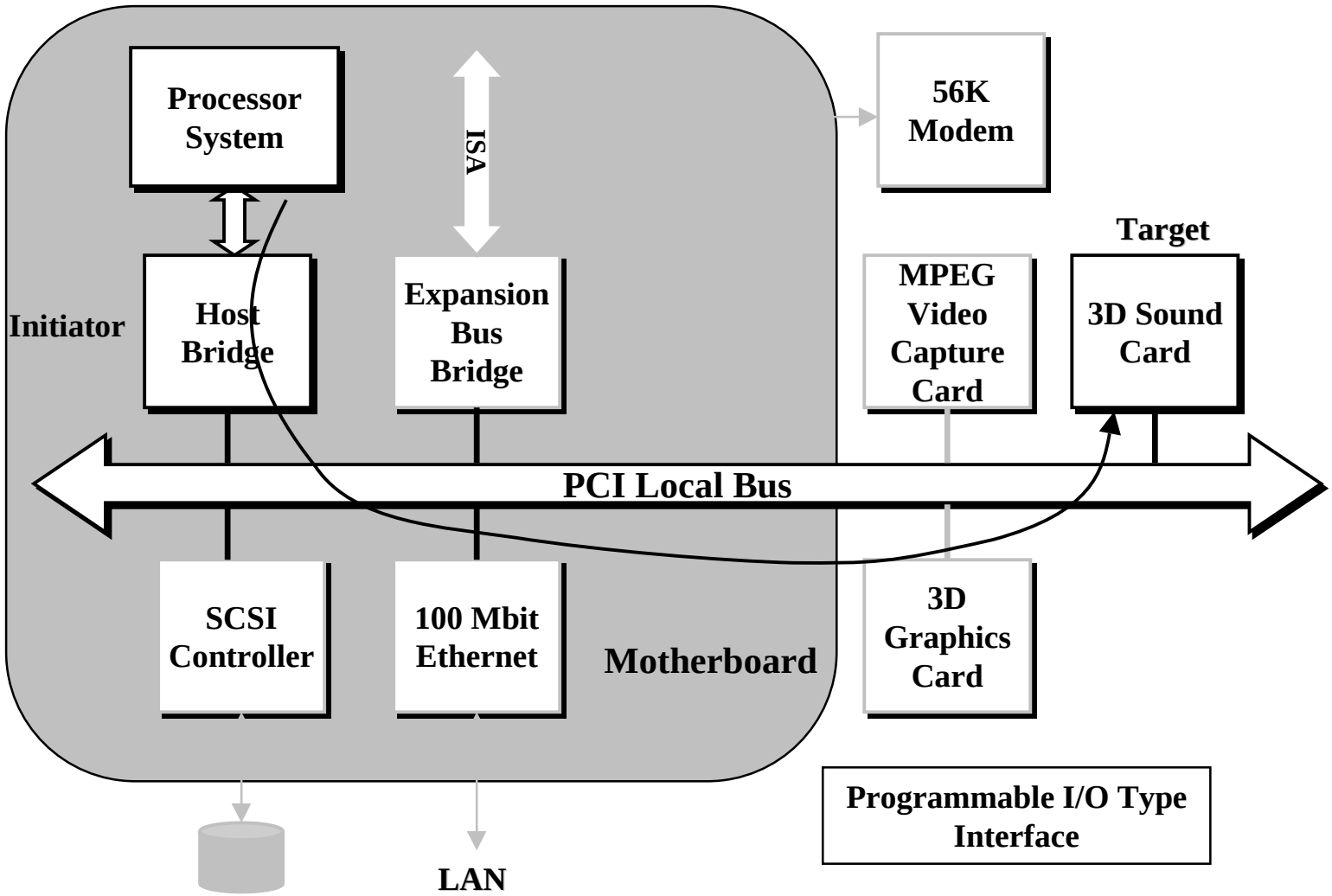
Sample Transaction – PIO



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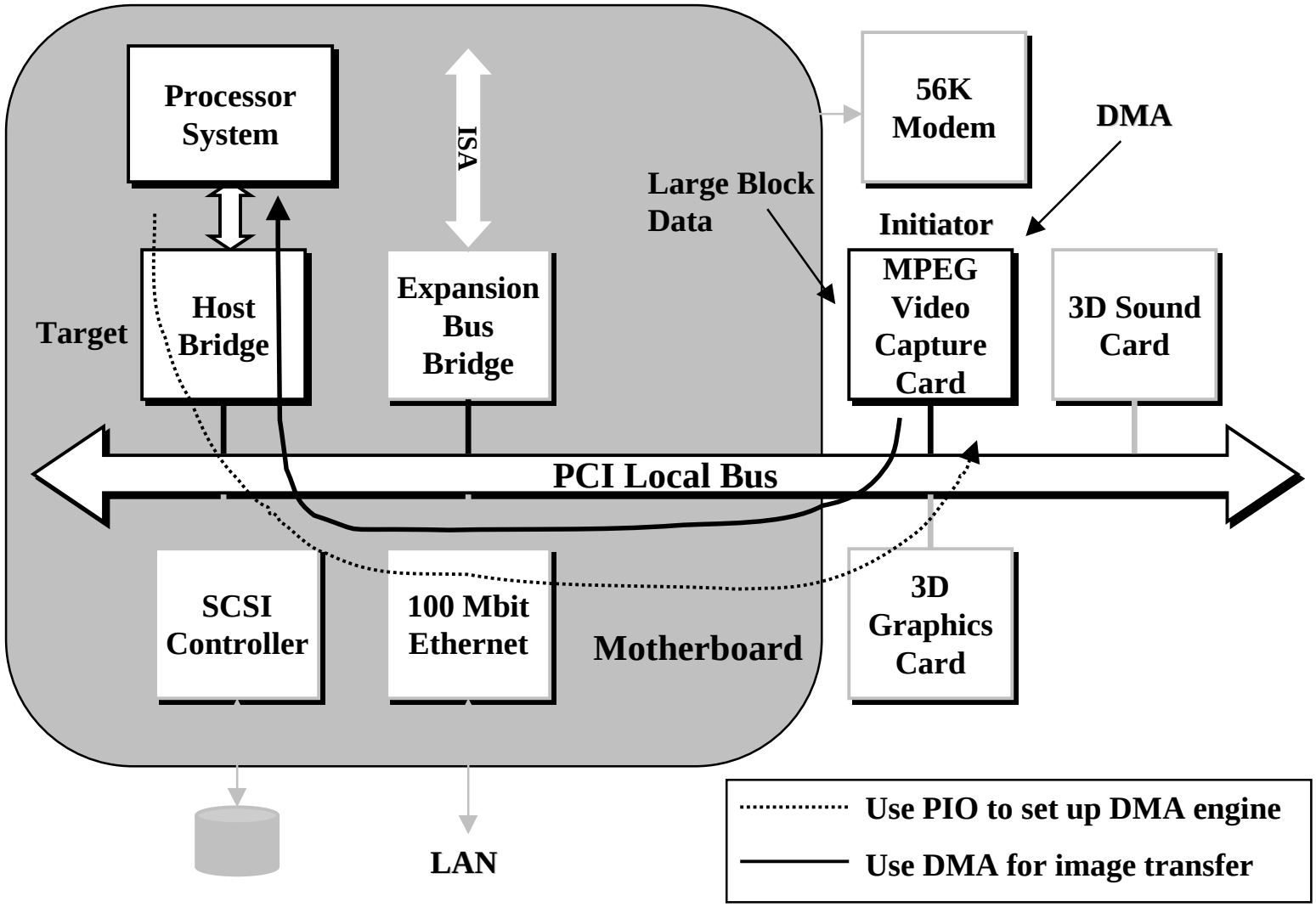
Sample Transaction – DMA



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Key Terms

- **Initiator**
  - *Or Master*
  - *Owns the bus and initiates the data transfer*
  - *Every Initiator must also be a Target*
- **Target**
  - *Or Slave*
  - *Target of the data transfer (read or write)*
- **Agent**
  - *Any initiator/target or target on the PCI bus*

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PCI Signals

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Clock and Reset

- **CLK**
  - *PCI input clock*
  - *All signals sampled on rising edge*
  - *33MHz is really 33.33333MHz (30ns clk. period)*
  - *The clock is allowed to vary from 0 to 33 MHz*
    - The frequency can change “on the fly”
    - Because of this, no PLLs are allowed
- **RST#**
  - *Asynchronous reset*
  - *PCI device must tri-state all I/Os during reset*

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Transaction Control
Initiator Signals

- **FRAME# – I/O**
  - *Signals the start and end of a transaction*
- **IRDY# – I/O**
  - *"I-Ready"*
  - *Assertion by initiator indicates that it is ready to send or receive data*

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Transaction Control
Target Signals

- **DEVSEL# – I/O**
  - *Device select*
  - *Part of PCI's distributed address decoding*
    - Each target is responsible for decoding the address associated with each transaction
    - When a target recognizes its address, it asserts DEVSEL# to claim the corresponding transaction

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Transaction Control
Target Signals

- **TRDY# – I/O**
  - *"T-Ready"*
  - *When the target asserts this signal, it tells the initiator that it is ready to send or receive data*
- **STOP# – I/O**
  - *Used by target to indicate that it needs to terminate the transaction*

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Transaction Control
Configuration Signals

- **Uses the same signals as the target, plus . . .**
- **IDSEL – I**
  - *"ID-Sel"*
  - *Individual device select for configuration – one unique IDSEL line per agent*
  - *Solves the "chicken-and-egg" problem*
    - Allows the system host to configure agents before these agents know the PCI addresses to which they must respond

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Address and Data Signals

- **AD[31:0] – I/O**
  - *32-bit address/data bus*
  - *PCI is little endian (lowest numeric index is LSB)*
- **C/BE#[3:0] – I/O**
  - *4-bit command/byte enable bus*
  - *Defines the PCI command during address phase*
  - *Indicates byte enable during data phases*
    - Each bit corresponds to a “byte-lane” in AD[31:0] – for example, C/BE#[0] is the byte enable for AD[7:0]

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Address and Data Signals

- **PAR – I/O**
  - *Parity bit*
  - *Used to verify correct transmittal of address/data and command/byte-enable*
  - *The XOR of AD[31:0], C/BE#[3:0], and PAR should return zero (even parity)*
    - In other words, the number of 1's across these 37 signals should be even

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Configuration Transactions

- **Are generated by a host or PCI-to-PCI bridge**
- **Use a set of IDSEL signals as chip selects**
  - *Dedicated address decoding*
  - *Each agent is given a unique IDSEL signal*
- **Are typically single data phase**
  - *Bursting is allowed, but is very rarely used*
- **Two types (specified via AD[1:0] in addr. phase)**
  - *Type 0: Configures agents on same bus segment*
  - *Type 1: Configures across PCI-to-PCI bridges*

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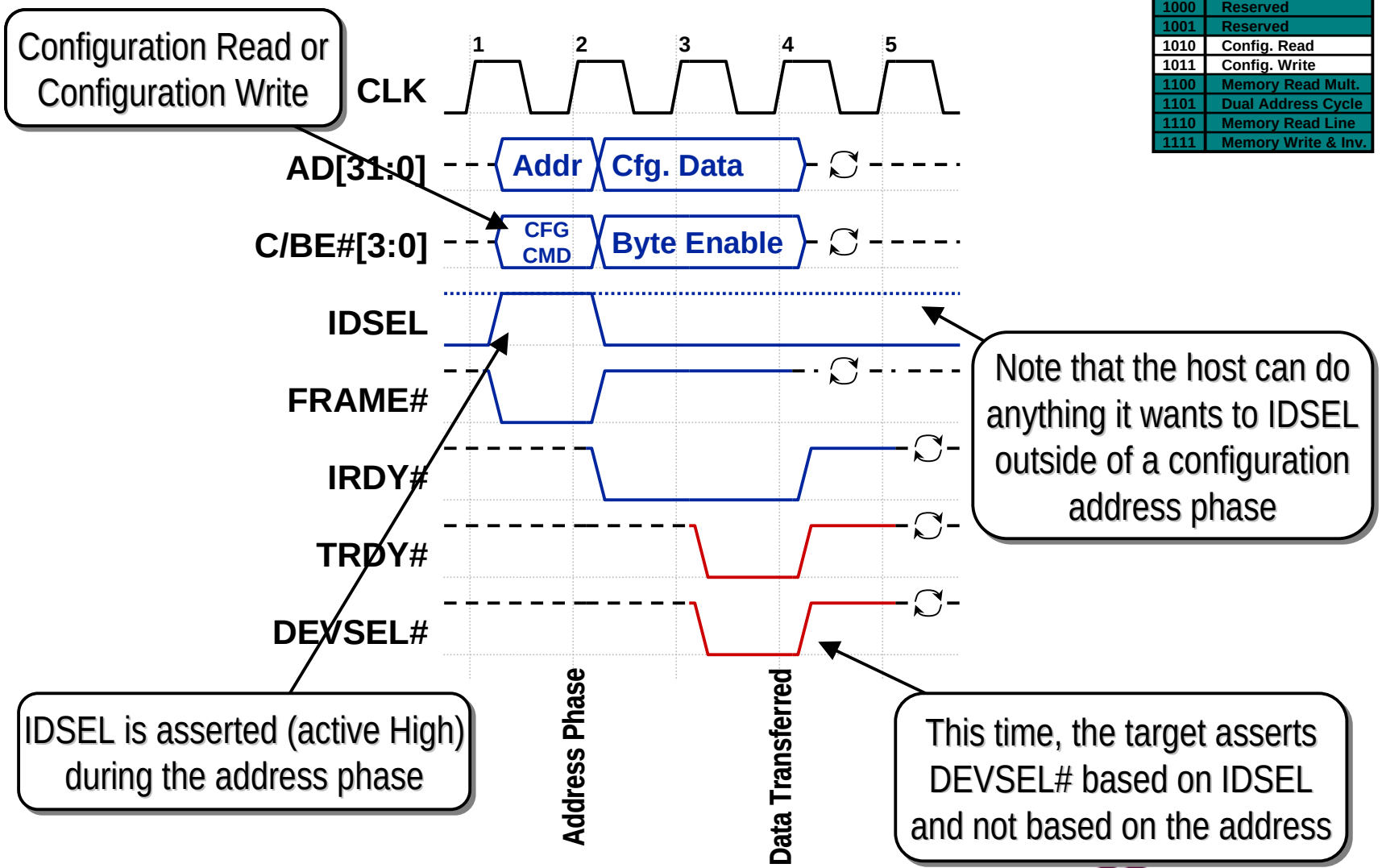
Configuration Example

C/BE#	Command
0000	Interrupt Ack.
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	Reserved
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	Reserved
1010	Config. Read
1011	Config. Write
1100	Memory Read Mult.
1101	Dual Address Cycle
1110	Memory Read Line
1111	Memory Write & Inv.



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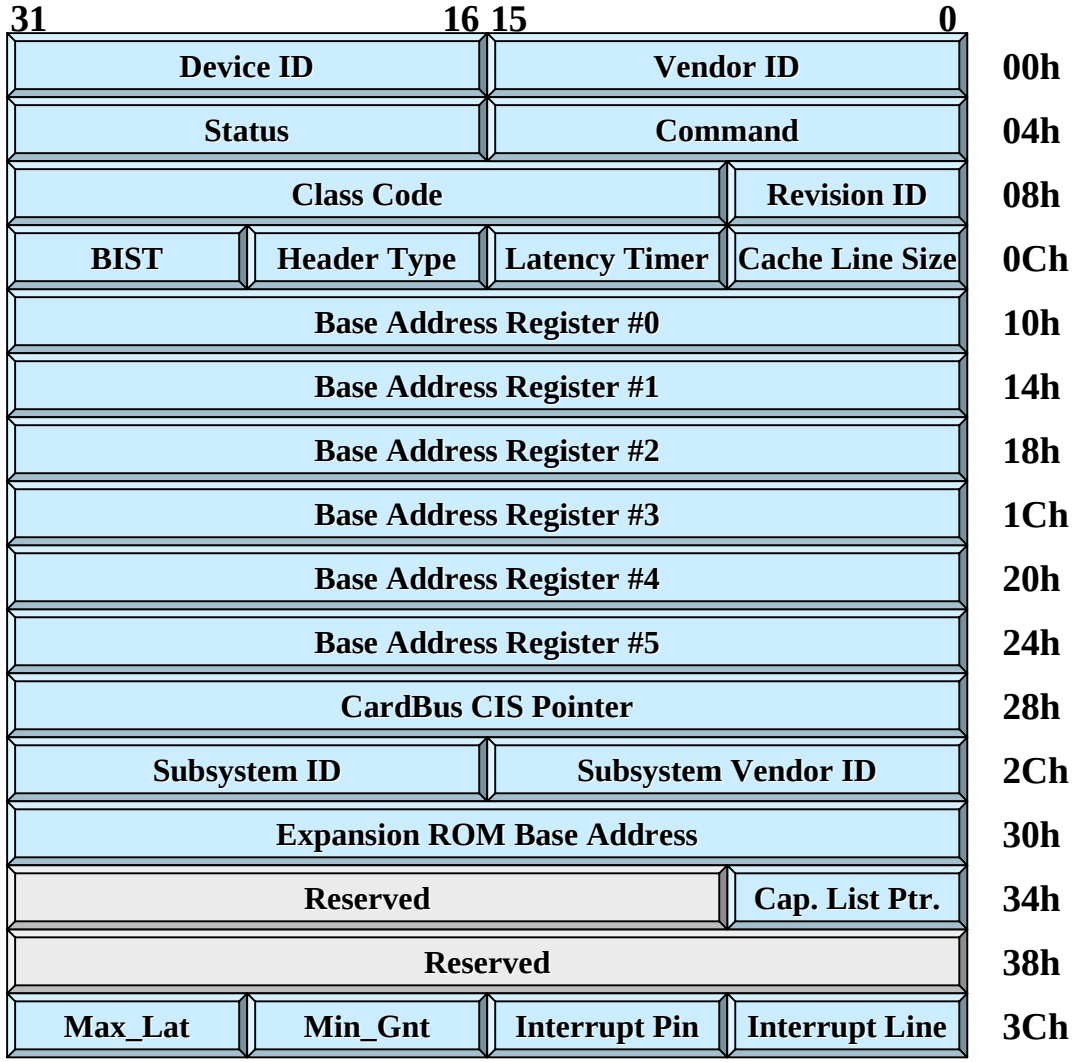
Standard PCI Configuration Header



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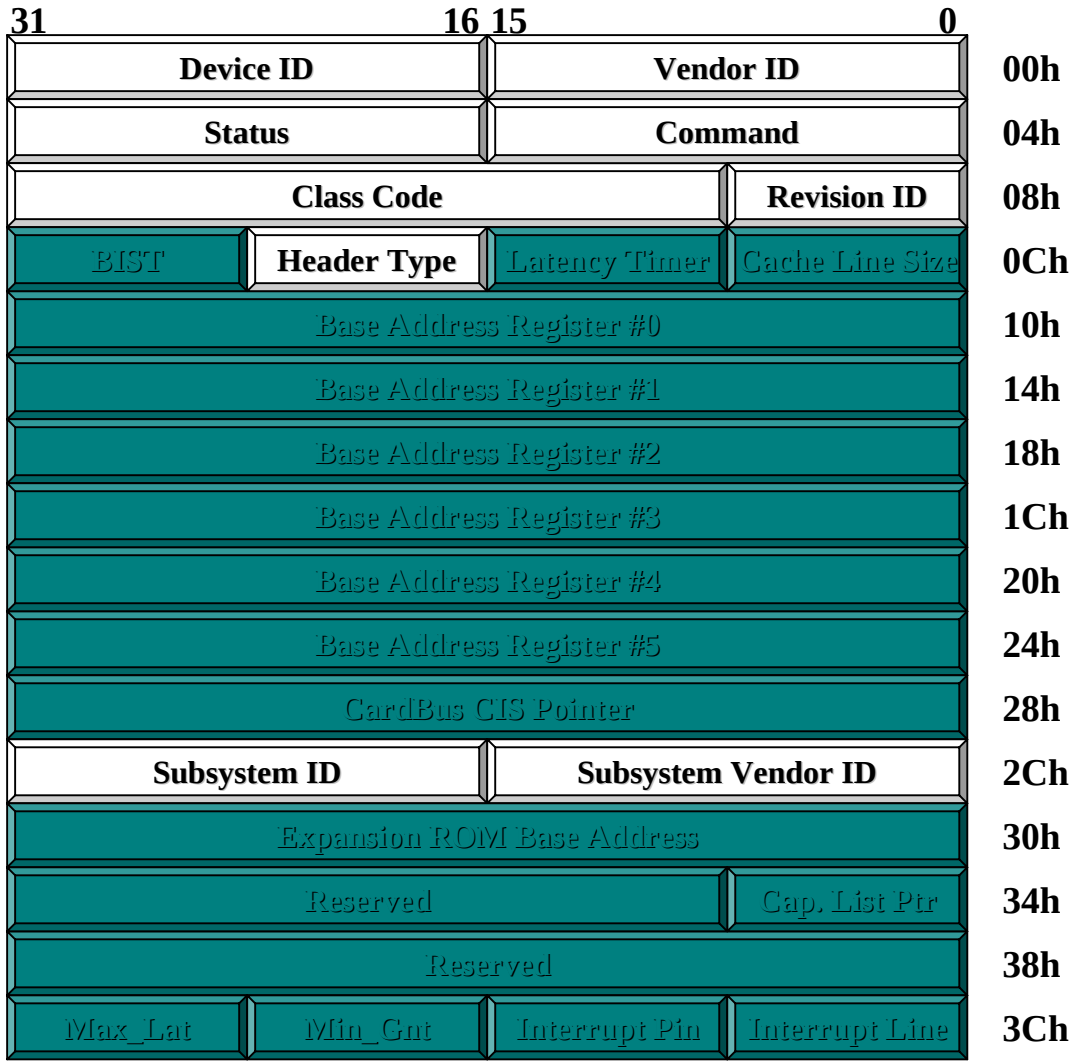
Required by PCI Spec 2.2



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Electrical & Timing Specifications

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Signaling Environments

- **The PCI spec describes two different electrical environments**
  - *5V signaling*
  - *3.3V signaling*
- **Technically, these names have *nothing* to do with the actual supply voltage**
  - *Rather, they are tied to logic-level thresholds*

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Signaling Environments

- **5V signaling is the most common**
- **66MHz PCI buses can only use 3.3V signaling**
  - *Note that 33MHz PCI can still use either*
- **Some plug-in cards can support both signaling environments – these are known as “universal” cards**

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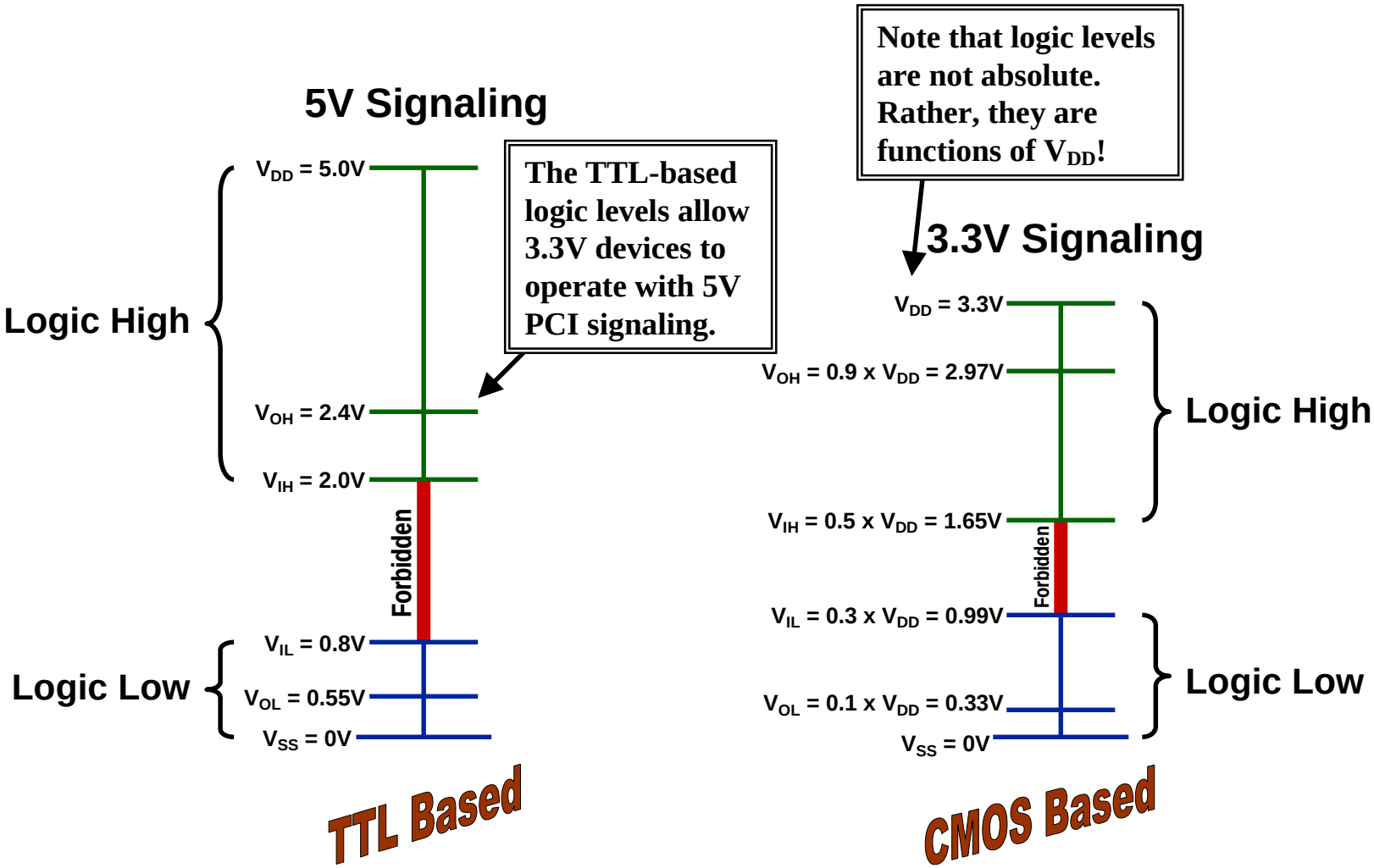
Signaling Environments



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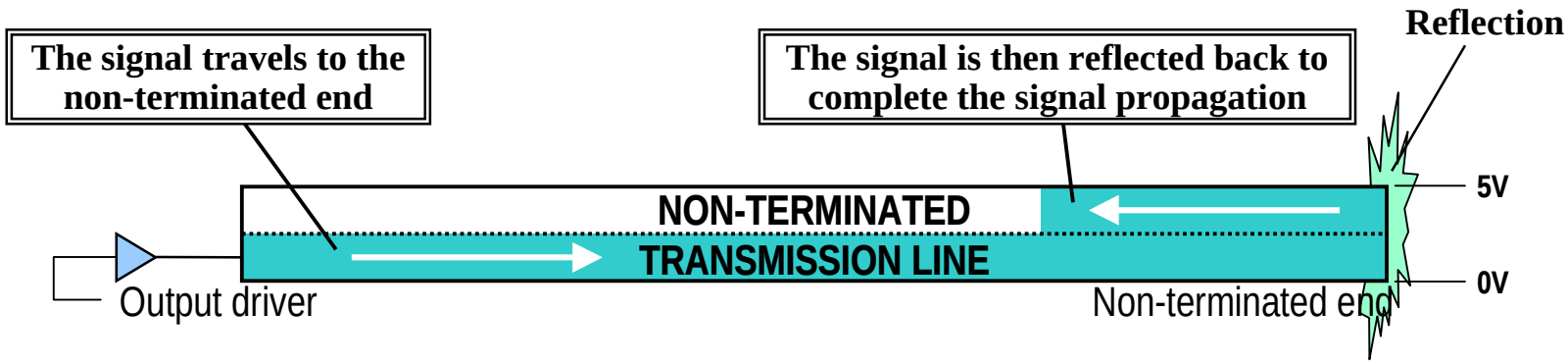
Reflective-Wave Switching

- **PCI uses “reflective waves”**
  - *Each wire on the PCI bus is a non-terminated transmission line, which causes signals to reflect over the length of the trace*
  - *Valid voltage levels are obtained after one reflection; this reduces the cost of PCI by not requiring high-powered output drivers*



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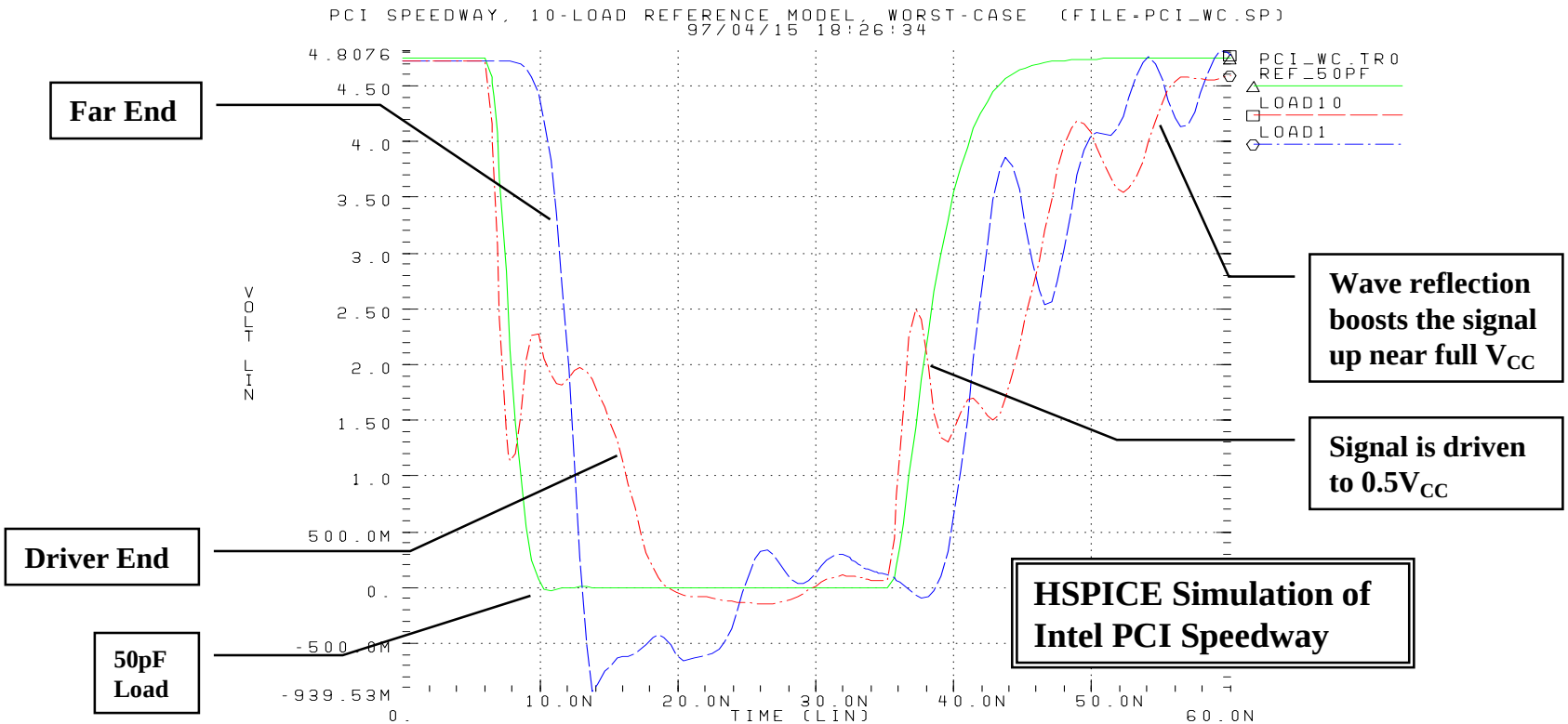
Reflective-Wave Switching

- This display shows how a reflection looks



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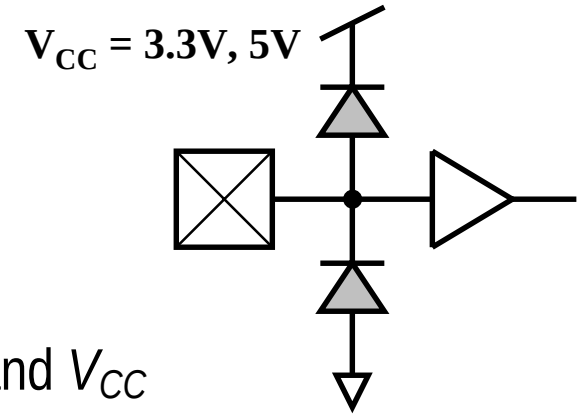
PCI – AC Specifications
Input Requirements – Clamp Diodes

- **Clamp diodes protect inputs from momentary short-circuit current caused by tri-stating delays**
- **5V signaling environment**
  - *Inputs must be clamped to ground*
  - *Upper clamp to 5V rail is optional*
- **3.3V signaling environment**
  - *Inputs must be clamped to both ground* and V_{CC}
  - *For universal cards (or any other 3.3V device that interfaces to 5V PCI), inputs must be clamped to the 5V supply, not the 3.3V supply*



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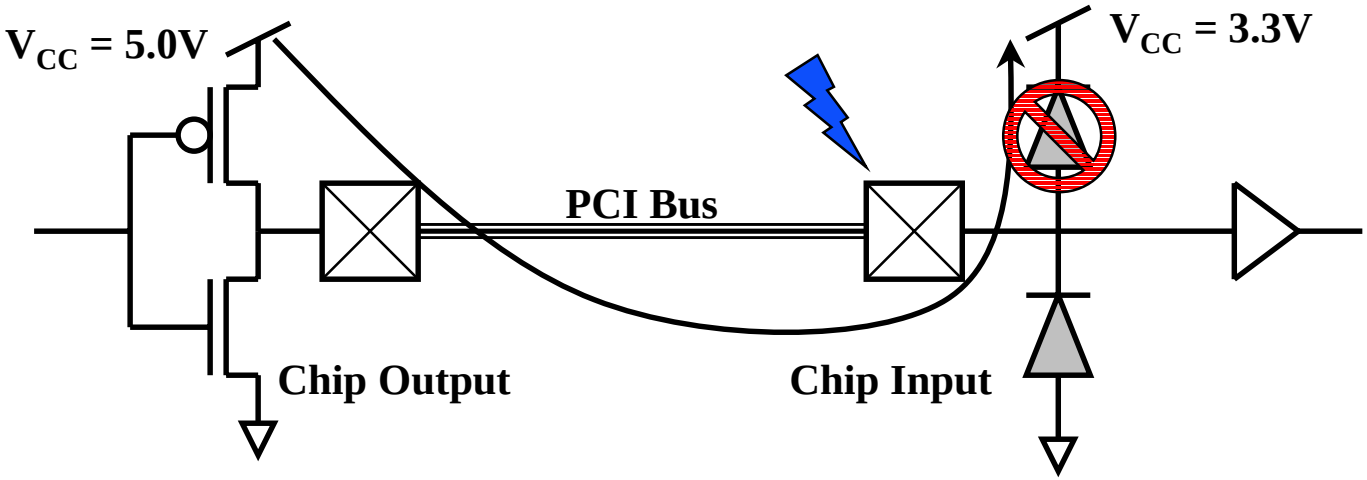
Bad Diode Clamping
Why Must Universal Cards Clamp to 5V?



- A universal card clamped to 3.3V, that is plugged into a 5V signaling bus, will create a short-circuit connection between the motherboard's 5V and 3.3V supplies!

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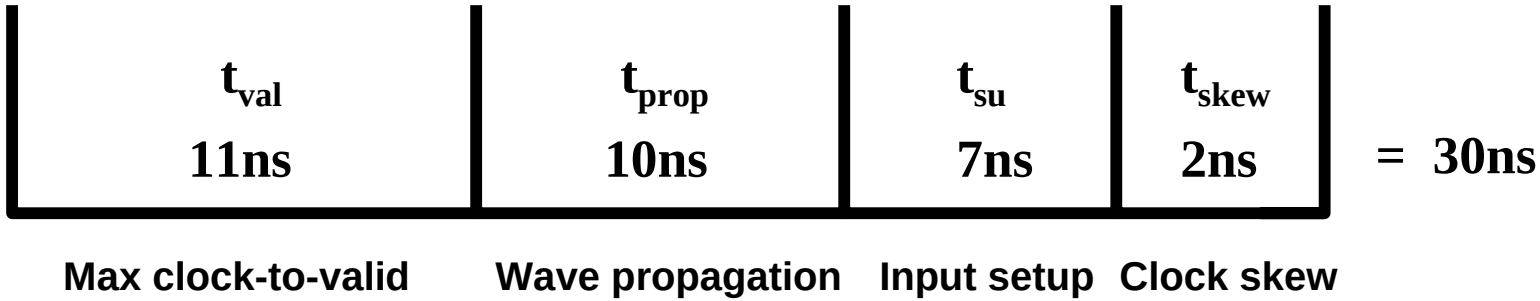
33MHz PCI Timing Specification

30ns Bus Cycle Time



Other Requirements:

Hold time : 0ns
Min clock-to-out : 2ns
Output off time : 28ns

All timing parameters are measured at the package pin

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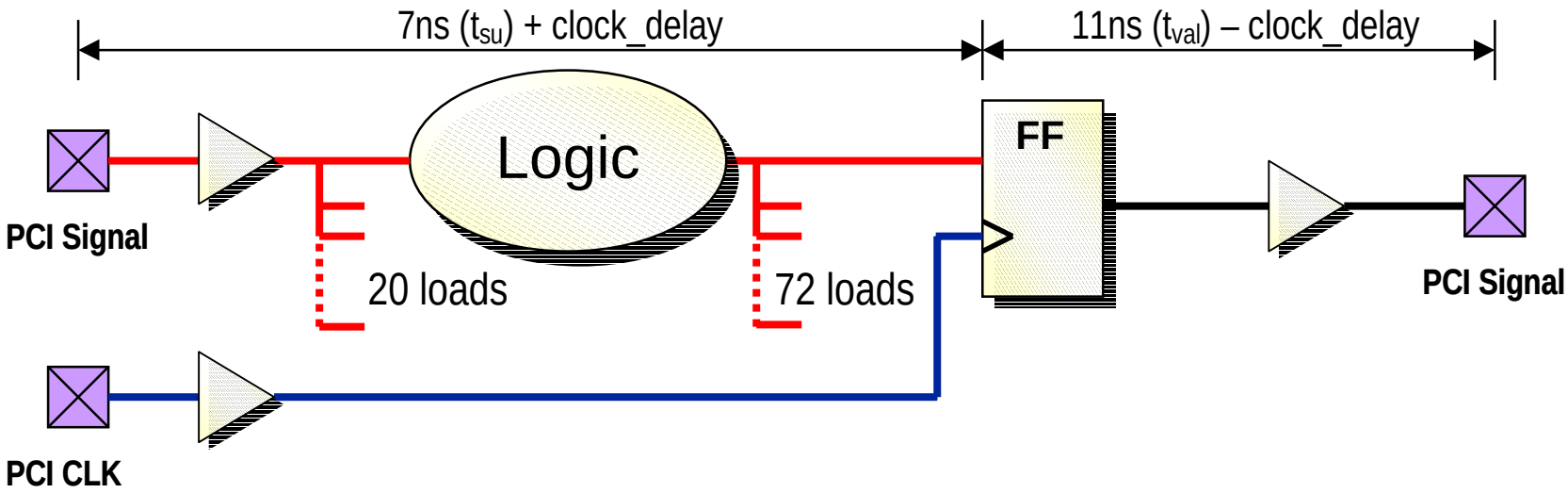
Why Is PCI Timing So Tough?



- **PCI handshaking performed every clock cycle**
  - *These signals* can't be pipelined
- **7ns setup + clock_delay → 100+ MHz! [33 MHz PCI]**
- **3ns setup + clock_delay → 220+ MHz! [66 MHz PCI]**

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Add-In Card Design

- **Trace length**
  - *All 32-bit PCI signals must be no more than 1.5″*
  - *All 64-bit ext. signals must be no more than 2.0″*
- **Clock trace must be exactly 2.5″ (± 0.1″)**
  - *Routed to only one load*
  - *Needed for clock-skew control*
- **PCI device requirements**
  - *One pin per signal!*
  - *Max input capacitance is 10pF (unless the device is on the motherboard, where 16pF is OK)*

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System Issues – Bus Loading

- **No PCI spec requirement as to the loading on the bus; however:**
  - *A driver must meet the 10ns propagation spec*
- **The rule of thumb is 10 loads max for 33MHz**
  - *Motherboard devices count as one load*
  - *Each add-in card slot counts as two load*
  - *Since most PC motherboards must have ≥2 PCI devices, they usually have no more than 4 slots*
- **More slots are available using PCI-to-PCI bridges or peer-to-peer PCI systems**

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64-Bit and 66MHz PCI

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The 64-Bit PCI Extension

- Doubles the available PCI bandwidth (keeping the clock frequency at 33MHz) to 264 MB/sec
- 64-bit PCI can use both 5V and 3.3V signaling
- Only used for memory transactions

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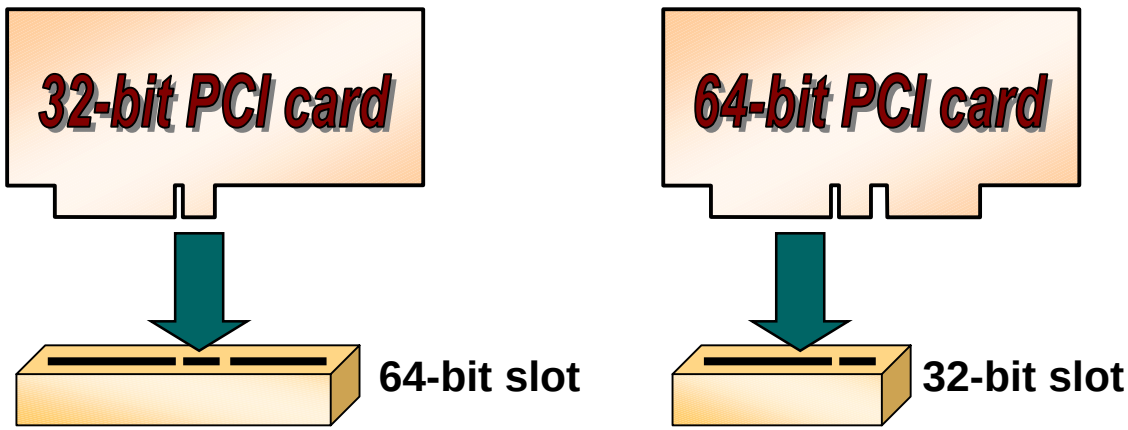
The 64-Bit PCI Extension

- **Mixing and matching is allowed**
  - *A 32-bit card can be plugged into a 64-bit slot*
  - *A 64-bit card can be plugged into a 32-bit slot*
  - *Use of the 32-bit vs. 64-bit datapath is negotiated between the initiator and target at the start of each transaction*



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Additional 64-Bit Pins

- **AD[63:32]**
- **C/BE#[7:4]**
  - *Used only for byte enables (not for PCI commands) except in the special case of Dual Address Cycle, discussed later*
- **PAR64**
  - *The XOR of AD[63:32], C/BE#[7:4], and PAR64 must equal zero (even parity)*

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Additional 64-Bit Pins

- **REQ64#**
  - *Mirrors FRAME# – indicates that the initiator requests a 64-bit transaction*
- **ACK64#**
  - *Mirrors DEVSEL# – indicates that the target is able to fulfill the transaction request using the 64-bit datapath*
  - *By not asserting ACK64#, the target tells the initiator that it is a 32-bit agent*

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64-Bit Initiator to 64-Bit Target

- **Works the same as a standard 32-bit transaction, with the following additions:**
  - *The initiator asserts REQ64# to mirror FRAME#*
  - *The target, in response, asserts ACK64# to mirror DEVSEL#*
- **Data is transferred on AD[31:0] *and* AD[63:32]**
  - *C/BE#[7:4] and PAR64 are also used*
- **The starting address must be QUADWORD aligned (i.e., divisible by 8: AD[2] = 0)**

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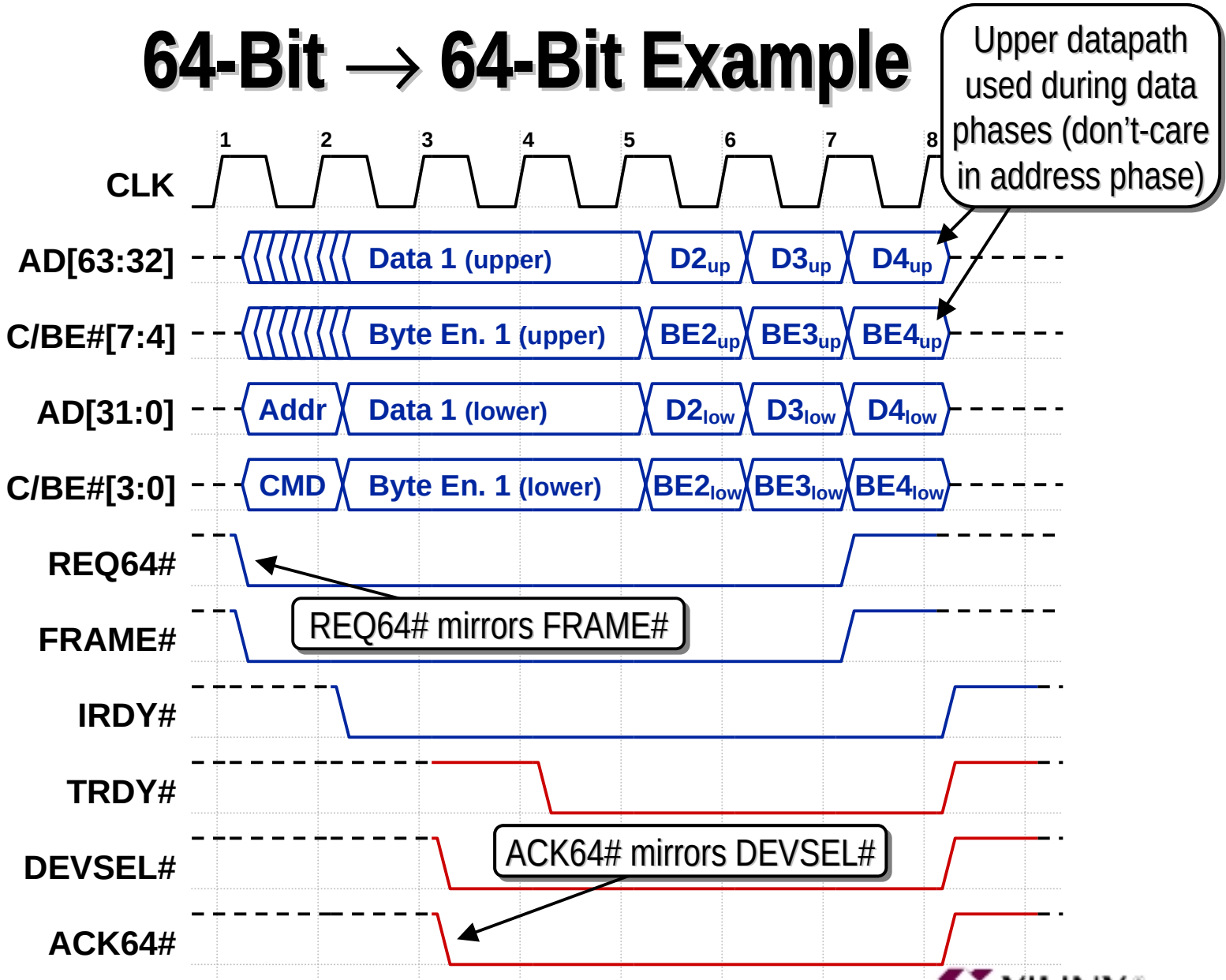
64-Bit → 64-Bit Example



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66MHz PCI Overview

- Pushes PCI bandwidth as high as 528MB/sec
- Most often used with the 64-bit extension, although it is legal to have 32-bit 66MHz PCI
- The signaling protocol is the same as with 33MHz PCI

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66MHz PCI Overview

- 66MHz PCI can only use 3.3V signaling
- A device that can operate at 66MHz has the 66MHz Capable bit set in the Status Register
- The loading allowance is cut in half (5 loads), so only one or two add-in slots are possible
- For open systems, 66MHz add-in cards must also work on a 33MHz PCI bus

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PCI Variations

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Overview of PCI Variations

- **As a well-defined standard, PCI and its various flavors have been widely adopted by many industries that require high-bandwidth data systems**
  - *Industrial computing*
  - *Datacom and telecom*
  - *Portable systems*
  - *Desktop systems*
- **Up-and-coming variations on PCI look to push its maximum bandwidth even higher**

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PCI Variations
Same Protocol (Different Form Factor)

- **PMC**
  - *PCI in a mezzanine form factor*
- **CompactPCI**
  - *PCI in a Eurocard (VME-style) form factor*
  - *Used as a passive backplane*
  - *Used in physically rugged environments such as industrial and telecom systems*
- **Mini PCI**
  - *New proposed PCI standard for portable systems*

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PCI Variations
Modified Protocol

- **CardBus**
  - *PCI in a PCMCIA form factor (portable systems)*
  - *Point-to-point, only slightly different protocol from standard PCI*
- **AGP (Advanced Graphics Port)**
  - *PCI-like point-to-point protocol*
  - *Primarily used for PC graphics cards*
- **PCI-X**
  - *New proposal to push bandwidth over 1GB/sec*
  - *Backward compatible with standard PCI*

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CompactPCI

- Used in Telecom and Industrial Applications that Require a Rugged Form Factor (Eurocard)
- IC Devices Maintain Specs from Standard PCI
- CompactPCI Imposes Additional Requirements for Add-in Cards as well as for the Host System
- Supports up to Eight Plug-in Slots
- Spec Maintained by the PCI Industrial Computer Manufacturers Group (PICMG), of which Xilinx is a Member

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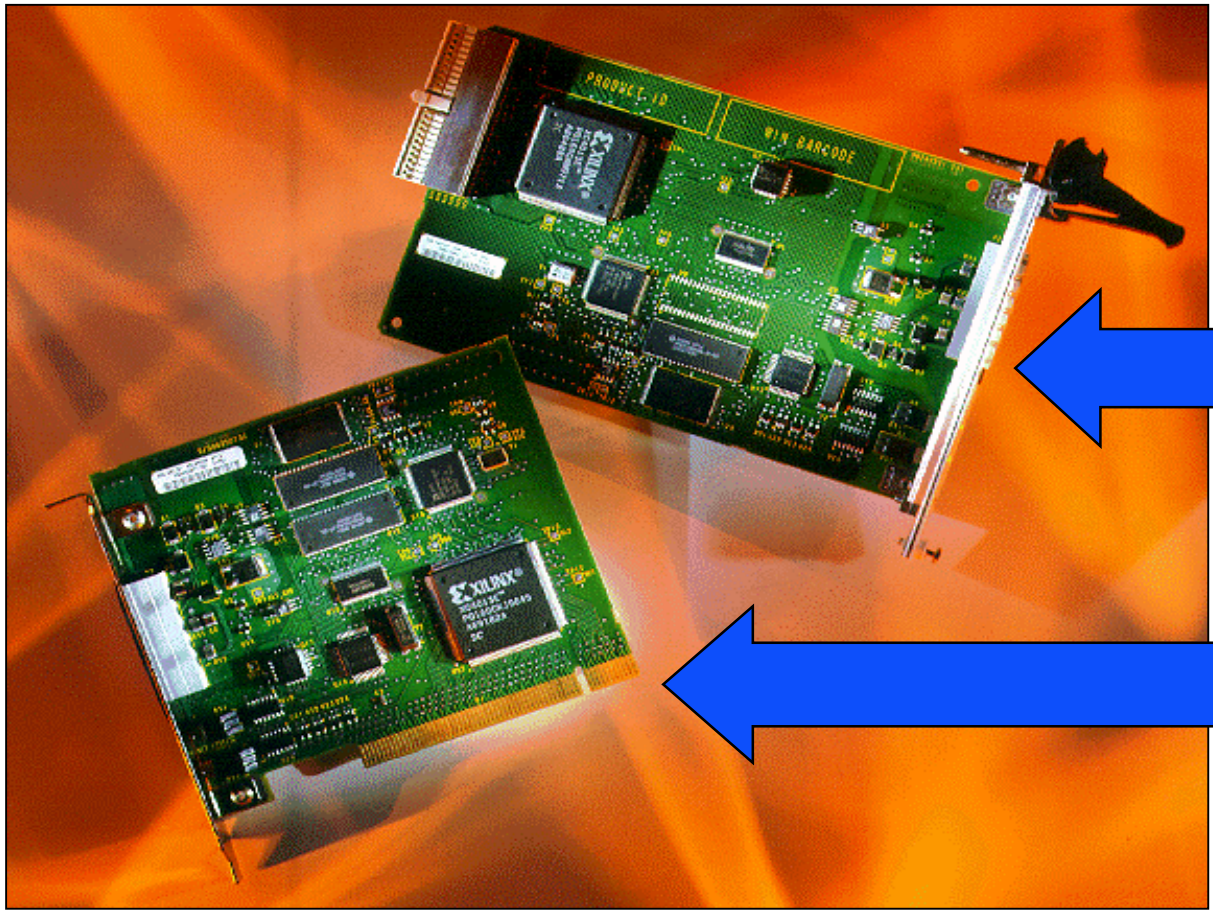
PCI / CompactPCI Comparison



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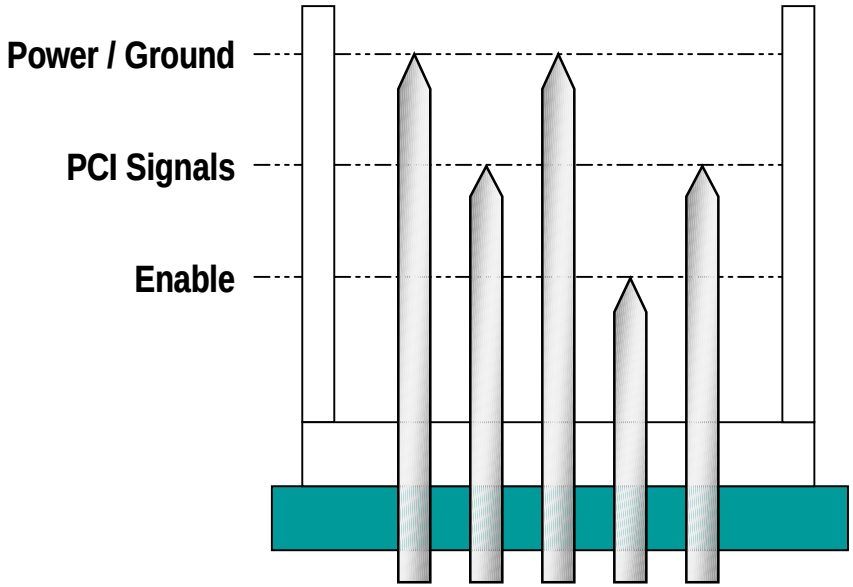
Hot-Swap CompactPCI

- **Live Insertion and Removal of Cards**
  - *High-availability systems (e.g., telecom)*
- **Electrical Issues**
  - *Signal lines need precharge to ~1V*
  - *Leakage current must be less than 10µA*
  - *Limited early power (2A maximum)*



Staged pins on backplane

- **Adds Hot-Swap Register to configuration space**
- **Not to be confused with Hot-Plug**

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Hot-Swap CompactPCI
Levels of Compliance

- **"Capable" – The Minimum Level of Compliance**
  - *Must be at least PCI v2.1 compliant*
  - *Must be able to tolerate precharge voltage (~1V)*
  - *Must be able to tolerate asynchronous RST#*
- **"Friendly" – The Intermediate Level of Compliance**
  - *Must at least be Hot-Swap "Capable"*
  - *Must also support the Capabilities List Pointer (PCI v2.2)*
- **"Ready" – The Highest Level of Compliance**
  - *Must at least be Hot-Swap "Friendly"*
  - *Must also support internal Bias Voltage and Early power*

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The Xilinx PCI Solution

The PCI Challenge

1. Must Guarantee Timing

- *Setup, Max, and Min*

2. Must Guarantee the Behavior

- *Now and in the future*

3. Must Meet Performance Requirements

- *Sustained throughput at 66MHz*

4. Must Meet Cost Target

- *Single-chip solution*

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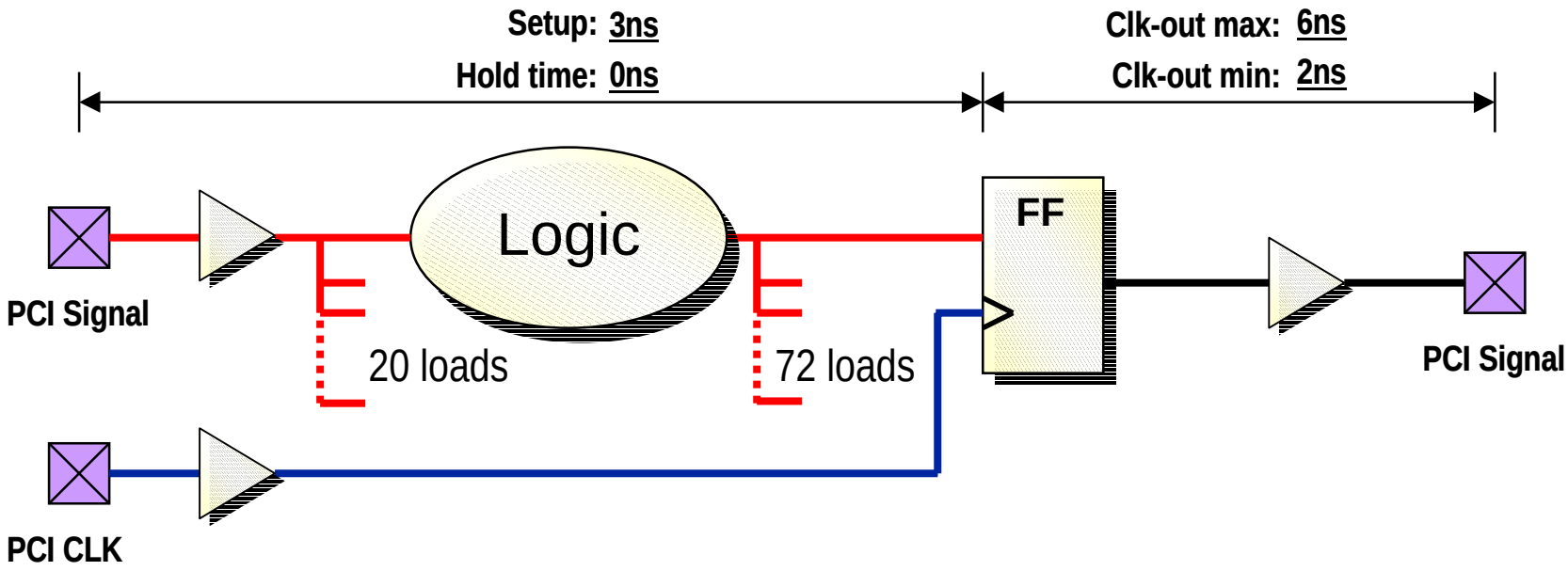
The PCI Challenge
The Critical Path



- The critical path is equivalent to **220+ MHz!**

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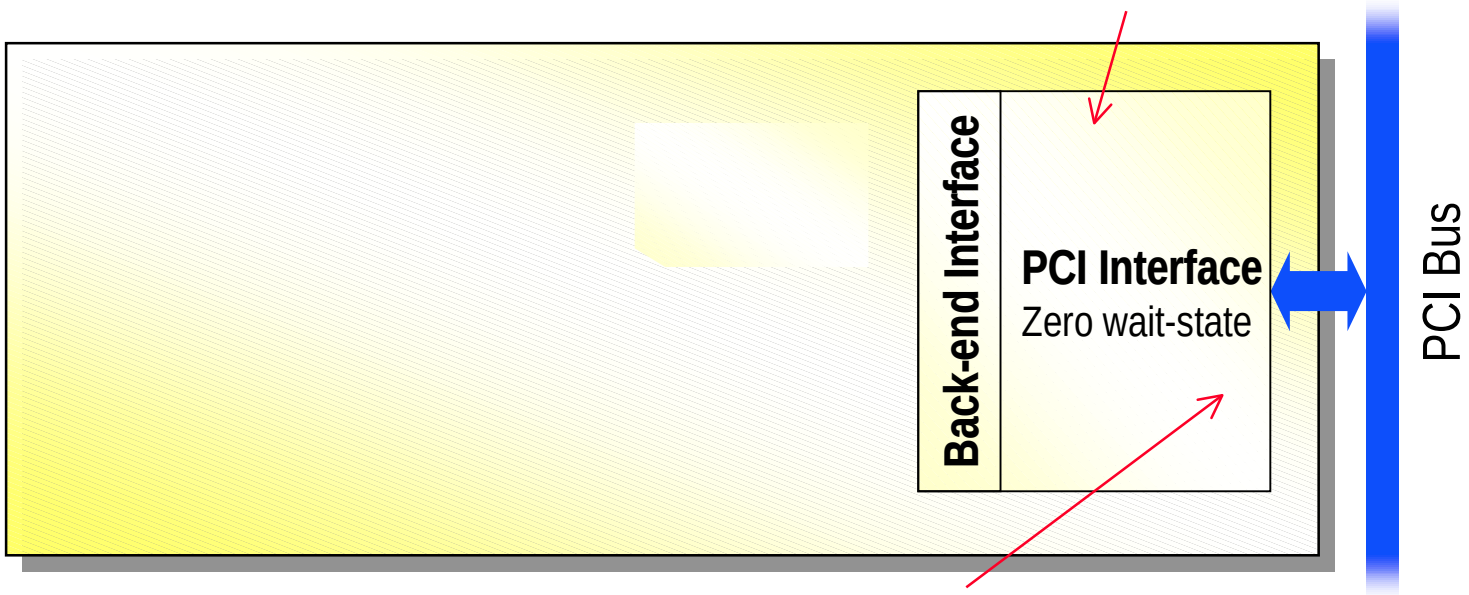

Real Performance

- Zero wait-state at 0-33MHz
- Full 32 or 64-bit data path

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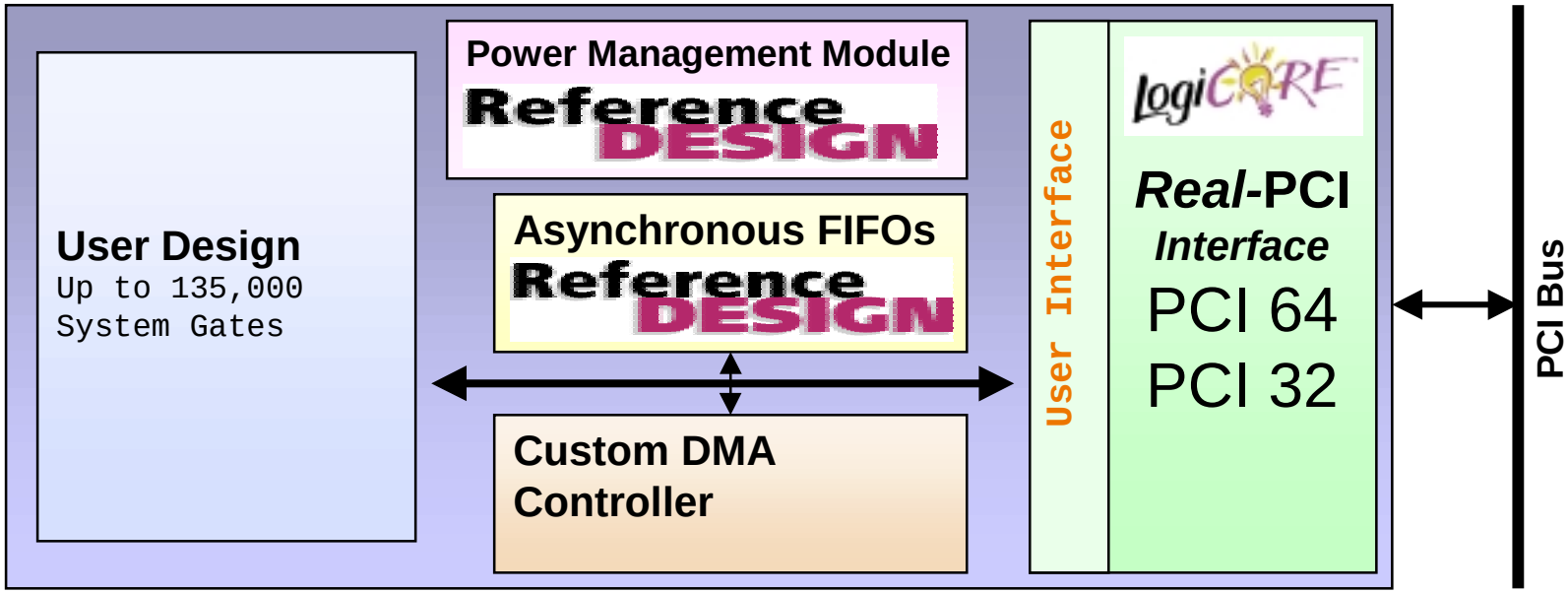
Supporting Reference Designs

- Asynchronous FIFOs & DMA Controller
- Power Management Module



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Extra Support from PCI Experts

- **Provide Worldwide Access to Certified PCI Experts that allow:**
  - *Support for targeting additional devices*
  - *Complete turnkey integration*

COMIT™ SYSTEMS

Memec Design Services

MULTI VIDEO DESIGN

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Ordering Information

	PCI64 Design Kit DO-DI-PCI64-DK	**PCI64** DO-DI-PCI64	**PCI32 Design Kit** DO-DI-PCI32-DK	**PCI32 Spartan** DO-DI-PCI32-S
Design File Access				
64-bit 66 MHz	Virtex-E Virtex	Virtex-E Virtex	-	-
64-bit 33 MHz	Virtex-E Virtex Spartan-II	Virtex-E Virtex Spartan-II	-	-
32-bit 33 MHz	Virtex-E Virtex Spartan-II Spartan-XL Spartan 4000XLA	Virtex-E Virtex Spartan-II Spartan-XL Spartan 4000XLA	Virtex-E Virtex Spartan-II Spartan-XL Spartan 4000XLA	Spartan-II Spartan-XL Spartan
Development Tools				
Prototyping board	Nallatech BallyLINX	-	VCC HotPCI	-
SW Driver Development Tools	NuMega SoftICE Driver Suite	-	NuMega SoftICE Driver Suite	-
Miscellaneous				
Reference Designs	PCI Bridge Designs Power Management	PCI Bridge Designs Power Management	PCI Bridge Designs Power Management	PCI Bridge Designs Power Management
Design Examples	Reference Drivers Board Gerber files)	-	Reference Drivers	-
PCI System Architecture Text Book	PCI System Arch Text Book Design Guide	Online	PCI System Arch Text Book Design Guide	Online

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The Xilinx PCI Design Flow

- The PCI Lounge
- Core Configuration and Download
- Simulation and Synthesis
- Implementation – Xilinx Alliance/Foundation

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The PCI Lounge

- **A Special Area for Xilinx PCI Customers on WebLINX**
  - *PCI core configuration and download*
  - *Latest design data – no CD required!*
- **To Gain Access, Customers Submit an Online Registration form**
  - *The customer selects a unique username and password*
  - *The customer also gives his or her product serial number as proof of purchase*

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PCI Lounge Registration

- **Register your LogiCORE product at:**

  http://www.xilinx.com/products/logicore/lounge/lounge.htm

- **During the registration process, you will be asked for:**
  - *Your LogiCORE product's serial number*
  - *Xilinx User ID and password (the same as your SmartAgent ID)*
    - You can create your own User ID during the registration process, if necessary
  - *The type of LogiCORE PCI Interface you purchased*

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PCI Lounge Registration

- In less than 2 business days, you will be sent a confirmation that you have access

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Downloading from the Internet

- **Once you are registered for the PCI Lounge, you can download your LogiCORE Interface in *two easy steps*:**
  1. *Customize your LogiCORE PCI Interface on WebLINX*
  2. *Download your tailor-made core*

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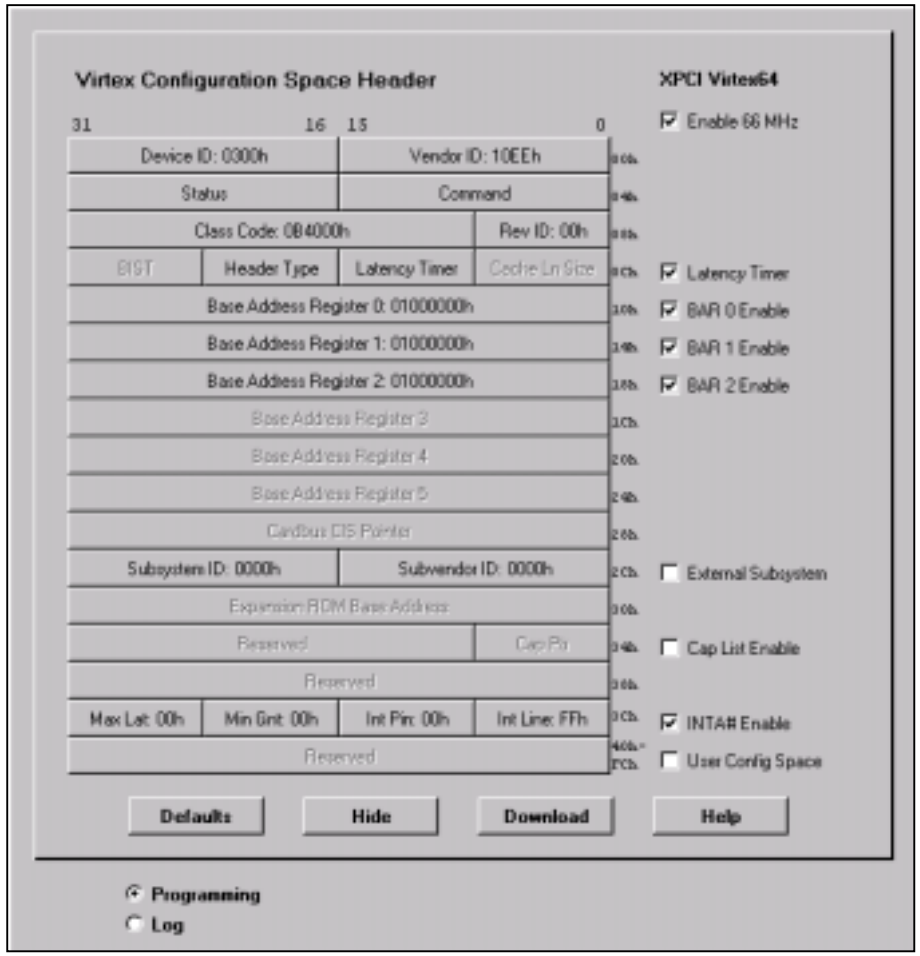
Downloading from the Internet

- **A Java-based GUI allows you to customize configuration options easily**
  - *See Chapter 3 of the* LogiCORE PCI User's Guide *for more detailed information*



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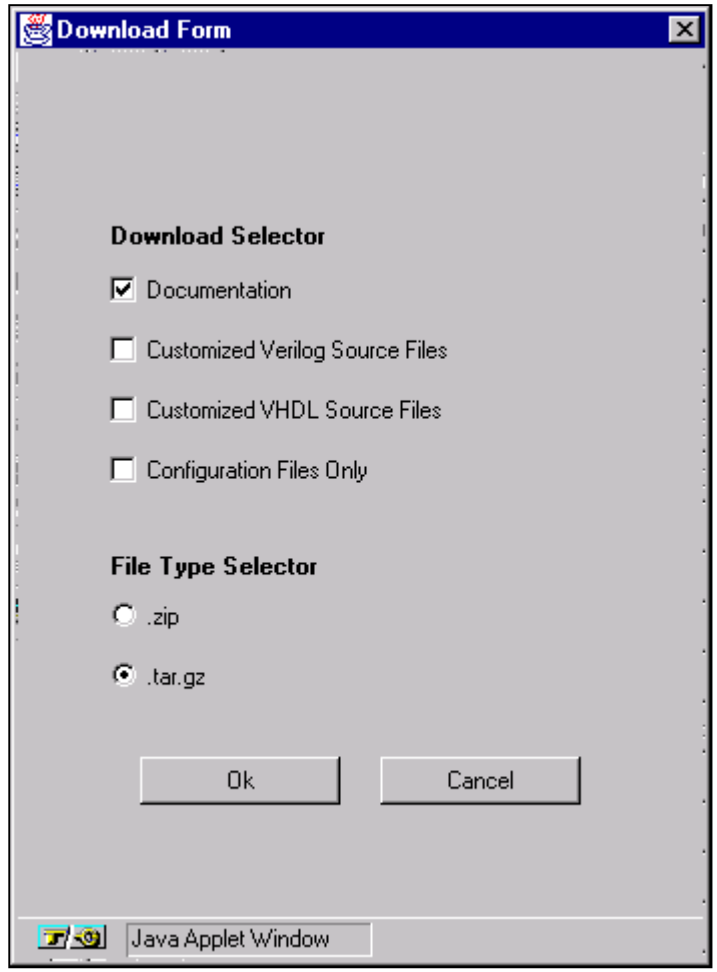
Downloading from the Internet

- **When it comes time to download, you can tailor the downloaded fileset for your design environment, based on:**
  - *Device and package*
  - *Design-entry tool*
  - *Archiving method*
    - .zip for PC
    - .tar.gz for Unix



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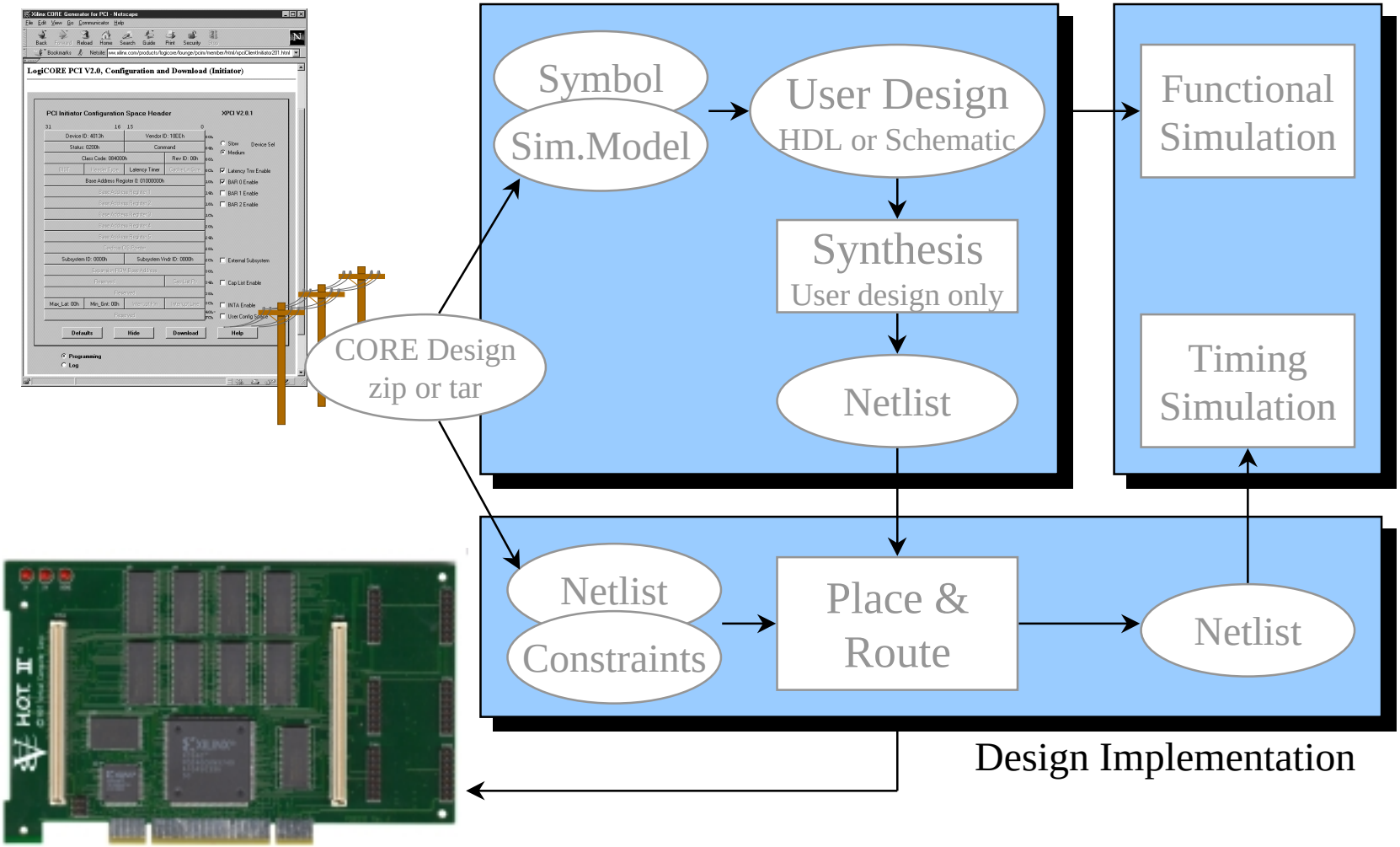
Xilinx PCI Design Flow Overview



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Simulation and Synthesis

- Functional and Timing simulation with -

- Synthesis with -

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XILINX®

Xilinx Implementation

- **Supported by Standard Xilinx Alliance and Foundation Series, V2.1i software**

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Available PCI Resources

- **LogiCORE PCI Lounges on WebLINX**
  - *www.xilinx.com/pci*
- **Xilinx Hotline**
  - *Expert PCI support engineers*
- **WWW based solutions and PCI Expert Journal**
  - *support.xilinx.com*
- **PCI-SIG discussion group**
  - *Mailing list subscription information on www.pcisig.com/forum.html*

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