HIPEG - A SINGLE CHIP MPEG-2 HDTV DECODER AND HIBOX - A DVB COMPLIANT HDTV DECODER BOX

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ABSTRACT

This paper describes one of the world's first single chip HDTV decoders according to the Main Profile@High Level of MPEG-2, called HiPEG. This chip has been designed by HHI within the European ACTS project CINENET and it is manufactured by Fujitsu using their advanced 0.35 µ technology. This chip is built into a DVB compliant HDTV decoder box, called HiBOX. This box accepts MPEG-2 transport streams and is therefore compliant with all DVB transmission systems such as DVB-S for satellite, DVB-C for cable or DVB-T for terrestrial transmission. During IBC this decoder box will be exhibited and it will be used for live DVB-T transmission of HDTV signals.

INTRODUCTION

High Definition Television has suffered from a lack of interest - especially in Europe - for some years. Nevertheless, HDTV technology has been used for some niche applications and due to the ongoing discussion in the U.S. and the recent decision of Japan, to introduce digital HDTV in the year 2000, the interest in Europe is growing again.

Recently HDTV became also an important issue within the European DBV project, since the acceptance of DVB standards outside Europe, and especially of DVB-T, is highly dependant on their suitability for HDTV transmission. Therefore the DVB project completed its „Implementation Guidelines for the Use of MPEG-2 Systems", which include now several HDTV formats. Furthermore, successful DVB-T transmissions of HDTV have been carried out in Australia at the end of 1997. In the meantime, the European ACTS project CINENET has been carried out after a two-year development of DVB compliant cable and satellite transmission systems as well as of high performance projectors for electronic cinemas using HDTV technology. Successful and very impressive live transmissions over satellite and cable have been demonstrated to the public in December 1997.

For this project one of the world's first single chip MP@HL HDTV decoders according to the MPEG-2 standard has been developed at HHI. This chip, called HiPEG, is manufactured by Fujitsu using their advanced 0.35µ technology. It supports all HDTV formats defined by DVB and furthermore all 18 ATSC formats. Furthermore, progressive output up to XVGA resolution is provided.

Additionally, HiBOX, an integrated HDTV decoder box, which is fully DVB compliant, has been developed. Besides power supply and connectors it consists of a single board, called HiBOARD, carrying six main building blocks, i.e. the systems demultiplexor, the audio surround sound decoder, the video decoder, a microcontroller, a DVB Common Interface, and the D/A converters for video and audio. These elements build up an MPEG-2 source decoder box with the following key features:

- Demultiplexing of Transport Stream data up to 280 Mbit/s
- Decoding of video data streams up to 80 Mbit/s and up to High Level resolution (1920 x 1152 pixels).
- Decoding of mulitchannel surround sound (MPEG-2 Surround Sound or AC3).
- Flexible controlling of demux and decoders to support various system configurations.
- Digital and analogue outputs for audio and video and digital output for data.
- Conditional Access to encrypted MPEG-2 Transport Streams.

HIPEG - A SINGLE CHIP MPEG-2 DECODER

HiPEG is a single chip that decodes MPEG-2 video data with the maximum allowed picture size of HDTV resolution. It decompresses the compressed data and produces synchronized digital output ready for digital-to-analogue conversion. The chip is programmable and supports various in/output formats, thus is ideal for online set-top box decoders for cable, satellite, terrestrial broadcast and offline applications like DVD or harddisk systems.

The Input Stream Handler (ISH) receives MPEG-2 encoded bitstreams either as Transport Stream (TS), Packetized Elementary Stream (PES) or Elementary Stream data (ES).

TS packets are unpacked to PES, whereas PES and ES are bypassed. In case of TS input the ISH makes PID-directed packet filtering, unpacking, PCRextraction, packet-loss detection and error-code insertion. In case of PES/ES error-code, insertion is controlled by an external signal. PES/ES data then is stored in an external SDRAM-FIFO (vbv_buffer). A FIFO-Controller (Fifocon) handles read/write actions, makes address computation and full/empty-flag generation. Buffer size and flags are programmable. An arbitration unit (Arbiter) organizes the sequence of read and write requests.

A general and simplified description of the data-flow within HiPEG is as follows (see Figure 1):

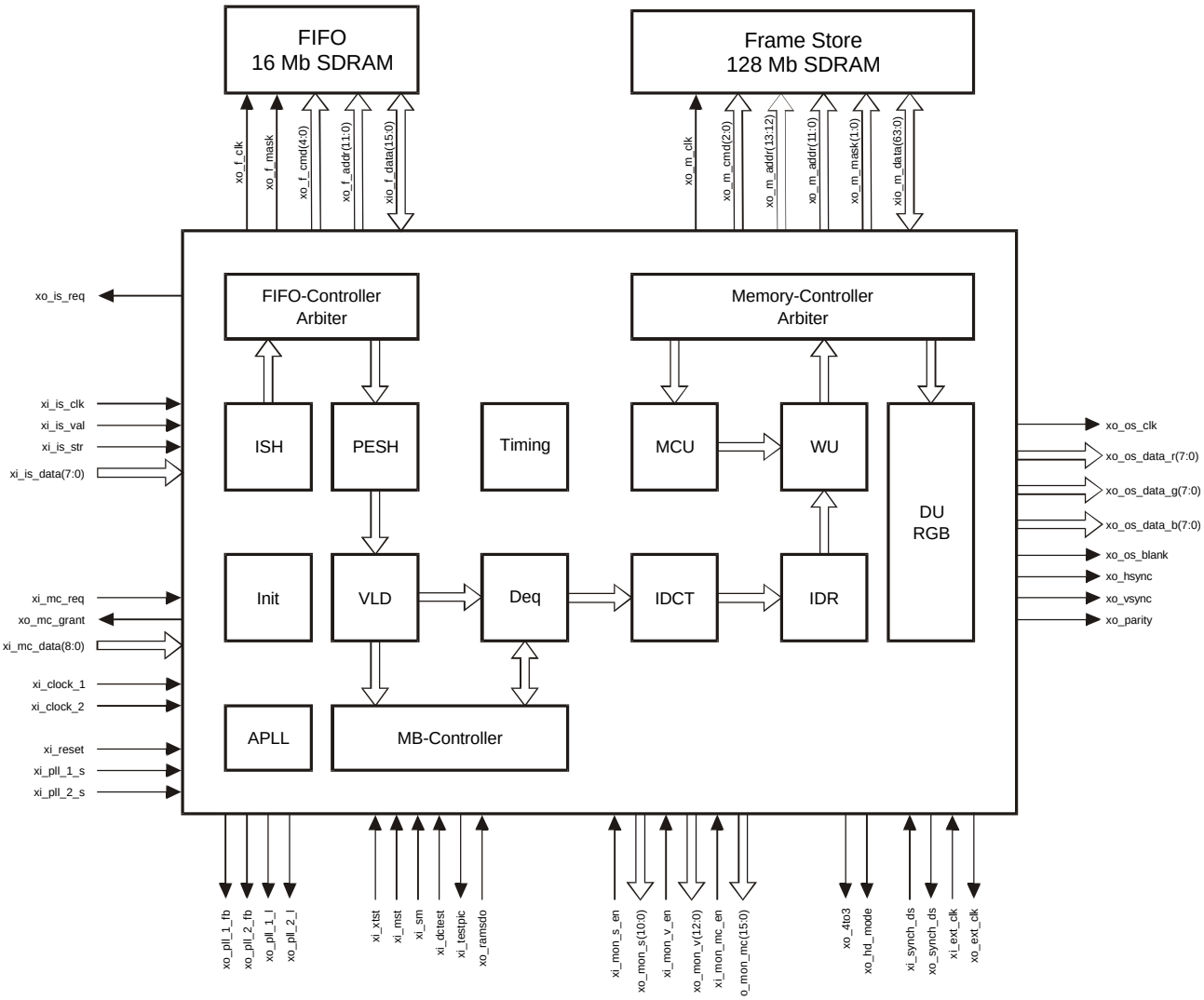


Figure 1. Block Diagram of HiPEG

In the next step PES/ES data is read from the external SDRAM-FIFO and transmitted to the Packetized Elementary Stream Handler (PESH). This unit unpacks PES to ES data or bypasses ES data to its output. In case of PES the time stamps PTS/DTS are extracted for synchronization of the decoding process.

The Variable Length Decoder (VLD) decodes the ES data and generates control information from the bitstream according to the MPEG video bitstream syntax and tables. Control information included in the various fields of the video bitstream is extracted as far as required and sent to the Dequantizer (Deq) and the Macroblock Controller (MBC).

The Timing unit controls the correct timing of the decoding process for this is essential for audio/video synchronization. In case of TS input, the Program Clock Reference PCR is received from the ISH and the Presentation/Decoding Time Stamp PTS/DTS is received from the PESH: Both values are used to compute the start time orf the decoding process. In case of PES + PCR input the PCR is delivered using the µ-controller bus via Init, whereas in case of ES input the value of vbv_delay is used for synchronization.

The Dequantizer performs zigzag scanning and inverse quantization on a block-by-block basis. Saturation and (IDCT) oddification is included in this unit. The output of the coefficients is sent to the Inverse Discrete Cosine Transformation unit (IDCT).

The Macroblock-Controller (MBC) receives all necessary picture and macroblock control information out of the bitstream and computes all necessary control information (e.g. motion vectors) on a macroblock by macroblock basis for the motion compensation backend of the decoder.

Before macroblock based motion compensation takes place the Inverse Discrete Cosine Transformation (IDCT) computes the frequency-to-spatial transformation on a block-by-block basis and passes the results to the backend. The Information Data Receiver (IDR) stores and reorders the IDCT output for motion compensation.

Motion vectors sent by the MBC addresses memory locations in the external frame store. Thus, the Motion Compensation Unit (MCU) performs motion vector based address computation, half-pel interpolation and interpolation of forward and backward reference macroblocks. The result of this process is stored in an on-chip macroblock memory.

Combining IDCT data (via IDR) with MCU data the Weighting Unit (WU) interpolates to the resulting reconstructed macroblock and stores it in the external frame store.

This frame store is build up by an internal Memory-Controller (MemCon) and an external SDRAM bank. Four frames (Actual, I-Picture, P-Picture, Ouput) are located in this memory for interpolation, reconstruction and output. Similar to the FifoCon the MemCon handles all three requests and produces command sequences for the SDRAMs.

The Display Unit (DU) grabs the decoded data from the SDRAM and prepares the data for output to a display. Major functions of this unit are the interpolation of 4:2:2 data out of the (decoded) 4:2:0 data, the interfacing of digital YUV/RGB in CCIR or HDI scheme, external synchronization and some picture editing capabilities. Progressive output and interlace-to-progressive transformation is supported too, as well as $YC_r C_b$ or RGB output.

The main features of HiPEG, which has a 3.3V voltage supply and about 2.5W power dissipation can be summarized as follows:

- Single-chip MPEG-2 HDTV video decoder
  - Supported profiles and levels: MP@ML, MP@H-14 and MP@HL
  - Decodes images up to 1920/1125/60/2:1 and 1920/1125/30/1:1
  - Supports all 18 ATSC and all DBV formats
  - Decodes I, P and B frames
  - General purpose interface for initialization & control
  - Self initialization
- Input interfaces
  - Supported input interfaces:
    - MPEG-2 Transport Stream (TS): DVB-SPI Interface, EN 50083-9
    - MPEG-2 Packetized Elementary Stream (PES): Synchronous/Asynchronous
    - MPEG-2 Elementary Stream (ES): Synchronous/Asynchronous
  - Input clock frequency up to 20.0 MHz
  - Input data rate up to 160.0 Mbps (exceeds MPEG requirements)
- Output interfaces
  - TV: ITU-R BT.601/656
  - H-14: Modified ITU-R BT.601/656 (Lum & Chrom parallel, 54.0 MHz)
  - HDTV: ITU-R BT.709/1120
  - Progressive output up to XVGA resolution
  - 4:2:0 to 4:2:2 to 4:4:4 conversion
  - Digital $YC_r C_b$/RGB output
  - 3:2 pull-down supported

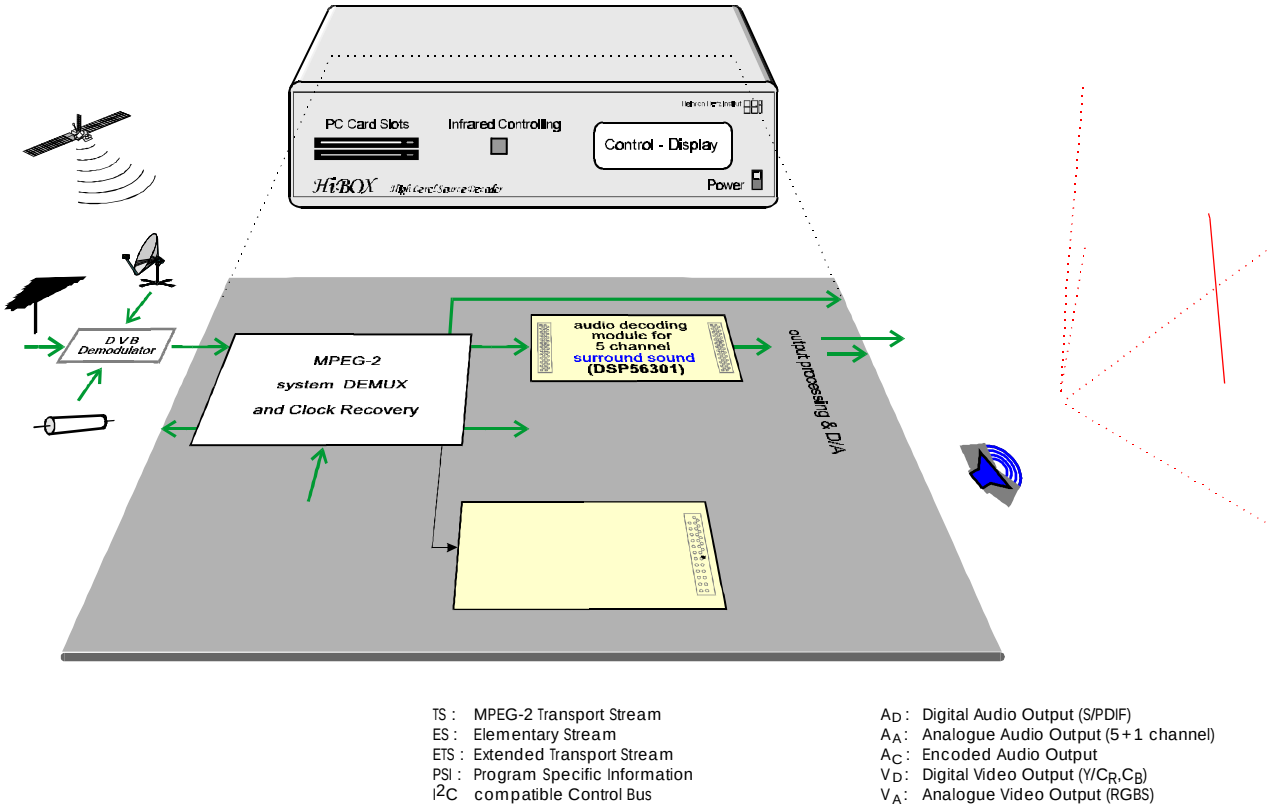
HIBOX - A DVB COMPLIANT HDTV DECODER BOX

An integrated HDTV decoder box, called HiBOX, which is fully DBV compliant, has been developed. Besides power supply and connectors it consists of a single board, called HiBOARD. This main board consists of six modules, which manage the signal processing starting from the MPEG-2 transport stream layer and ending at the analogue streams for presentation.

The following six blocks have been implemented:

- System demultiplexer including the system time clock recovery
- HDTV video decoding module including HiPEG
- Audio surround sound decoding module
- Output processing including D/A conversion
- Board controlling module KOLIBRI
- Module Joker for DVB Common Interface

Figure 2 gives a simplified overall view of the configuration and interfaces required for this purpose.



TS : MPEG-2 Transport Stream
ES : Elementary Stream
ETS : Extended Transport Stream
PSI : Program Specific Information
I^2C compatible Control Bus

A_D : Digital Audio Output (S/PDIF)
A_A : Analogue Audio Output (5+1 channel)
A_C : Encoded Audio Output
V_D : Digital Video Output ($Y/C_R,C_B$)
V_A : Analogue Video Output (RGBS)

Figure 2. HiBOX - DVB compliant High Level Source Decoding Box

The main functions of the MPEG-2 system Demux are to recover the System Time Clock (STC, 27 MHz) by the program clock reference (PCR) and to analyse the Program Specific Information (PSI), which is necessary for the demultiplexing procedure.

The audio decoder is implemented as software, running on a DSP. Both MPEG-1 stereo and MPEG-2 five channel surround sound are supported.

HiBOARD accepts MPEG-2 Transport Streams as input signals, which can be fed in either by the DBV Common Interface, where Conditional Access and descrambling can be implemented or by a DVB Professional Interface.

The output processing unit manages the video and audio interfacing according to several ITU-R standards.

The controlling unit board is used for diagnostics an dto load or modify system parameters. If no external system control over an I^2C connection is available, the system can be configured via switches, which trigger the software running on the control unit.

CONCLUSION

In this paper a complete decoder box HiBOX for compressed HDTV signals according to the MPEG-2 MP@ML standard has been presented. This decoder box is built around HiPEG, one of the world's first single chip HDTV video decoders for image resolutions up to 1152 lines x 1920 pixels. This chip is very flexible and it supports all TV and HDTV formats defined by DVB and by the ATSC. HiBOX is fully DVB compliant and can therefore decode compressed HDTV-signals which are transmitted via satellite (DVB-S), cable (DVB-C) or terrestrial transmitters (DVB-T).

HiBOX is based on a modulated concept and is therefore very flexible in its applications and configurations.

The box has all necessary hardware components for conditional access and descrambling. For audio, stereo as well as five channel surround sound are supported. By exchanging the video module the box can be used for stereo TV by decoding and synchronizing two separate MPEG-2 encoded video scenes representing a left and a right view of a stereo pair.

The system has been tested with over the air transmission of HDTV signals using a DVB-T modem. HIBOX will be demonstrated during IBC '98 at the joint booth of several European ACTS projects.